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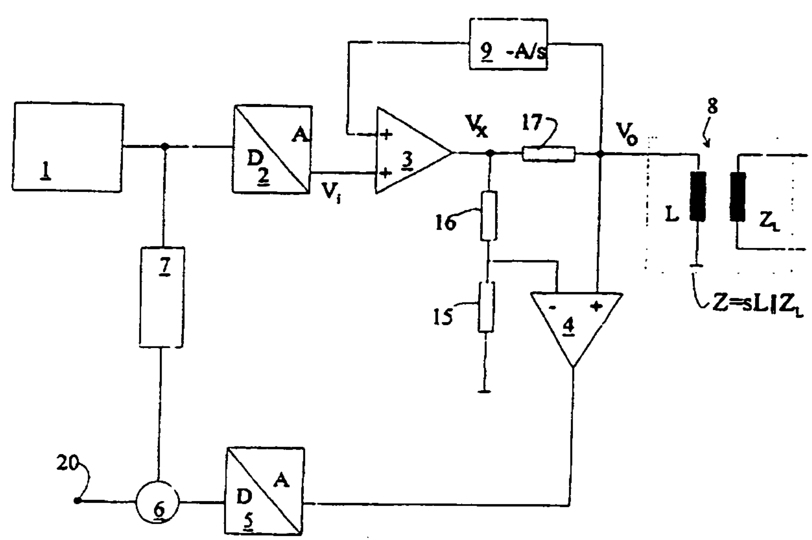

(57) Abstract

The invention relates to a circuit configuration and a method for adapting an echo-cancelling multispeed modem to a line. The circuit configuration comprises a transmitter (1), a transmitter buffer (3) connected on the signal path of the transmitter (1), a line drive resistance (17) connected to the output of the transmitter buffer (3), a line transformer (8) connected to the line drive resistance (17), and echo-cancelling elements (5, 6, 7) for eliminating the transmit signal echo from the receive signal. According to the invention, to the input of the transmitter buffer (3) is arranged a feedback path from the connection point of the line transformer (8) and the line drive resistance (17) by means of an integrator (9).

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MULTISPEED MODEM WITH ECHO-CANCELLING BY MEANS OF AN INTEGRATOR IN A FEEDBACK PATH

The present invention relates to a circuit configuration according to the preamble of claim 1 for adapting an echo-cancelling modem to a line.

The invention also concerns a modem adaptation method.

Conventionally, a modem is connected to a line via a transformer which isolates the line galvanically from the modem and serves as an overvoltage protection against transients imposed on the modem from the line. The transformer inductance of an echo-cancelling modem must be held within certain limits in order to keep the number of weighting coefficients of the digital echo-cancelling circuit sufficiently small as evaluated against to the implementation costs of the echo canceller, and on the other hand, to prevent the transformer from imposing excessive distortion on received signal, thus deteriorating the function of the modem receiver circuitry. In the prior art, adjustment of the transformer inductance has been problematic in multispeed modems, wherein the selection of an optimal inductance for each data transfer speed has required the use of, e.g., multiwinding transformers as well as relay or switch control circuits thereof.

It is an object of the present invention to overcome the drawbacks of the above-described technique and to provide

an entirely novel type of circuit configuration for adapting an echo-cancelling modem to a line.

The goal of the invention is achieved by providing with the help of an integrator in front of the transformer a feedback circuit in which, by virtue of a controlled time constant, the line transformer inductance can be adjusted dynamically according to the instantaneous data transfer speed using, e.g., a simple switched resistor matrix.

More specifically, the circuit configuration according to the invention is characterized by what is stated in the characterizing part of claim 1.

Furthermore, the method according to the invention is characterized by what is stated in the characterizing part of claim 9.

The invention offers significant benefits.

The digital circuit section associated with echo cancellation can be fabricated at a lower cost. The transformer matching circuit is realized without expensive multi-winding transformers and relay circuits required for their switching arrangements that are both costly and prone to malfunction.

In the following, the invention will be examined in greater detail with the help of exemplifying embodiments illustrated in the appended drawings in which

Figure 1 shows the block diagram of a circuit configuration according to the prior art;

Figure 2 shows the block diagram of a circuit configuration according to the invention;

Figure 3 shows a detail of the circuitry of Fig. 2; and

Figure 4 shows an alternative implementation of the circuit detail of Fig. 2.

Referring to Fig. 1, conventionally the signal from the transmitter 1 of an echo-cancelling multispeed modem is taken to a digital/analog converter 2, after which the analog output signal is buffered by a buffer amplifier 3, called the transmitter buffer. The circuitry, which comprises an isolation amplifier 4, impedances 15, 16 and 17 as well as the impedance $Z = sL \| Z_L$ formed by the transformer 8 and the line, perform in an echo-cancelling modem as a conventionally used hybrid circuit which cancels a portion of the reflected echo of the transmit signal (s denotes the variable of Laplace transform). The hybrid acts as a Wheatstone bridge, where the impedance 16 connected at its one end to the transmitter buffer 3 and the impedance 15 connected between the first impedance and the ground form the other branch of the bridge, while the impedance 17 connected at its one end to the transmitter buffer 3 and the impedance $sL \| Z_L$ formed together by the transformer 8 and the line perform as the other branch of the bridge. The impedance 17 connected

between the transmitter buffer 3 and the transformer 8 may also be called the line drive impedance. The hybrid attenuates the transmit signal echo the better the closer the impedance 15 is the resultant impedance of the transformer and the line, that is, the parallel connected impedance $sL\|Z_L$ of the main impedance L of the transformer 8 and the line impedance Z_L. Both the receive signal and the residual transmit signal echo are taken from the amplifier 4 for digitization to the analog/digital converter 5. While the above-described hybrid configuration is representative to a conventional embodiment, other circuit embodiments implementing the transfer function corresponding to the bridge branch formed by the impedances 15 and 16 may be contemplated without compromising performance of the invention.

As the parallel-connected impedance $sL\|Z_L$ of the transformer 8 and the line form one of the bridge impedances, the magnitude of the inductance L of the transformer 8 has such an effect on the transmit signal echo that if the transformer inductance is too high, the duration of the echo path impulse response (echo tail) increases from a normal situation, whereby efficient echo cancellation requires a greater number of weighting coefficients in the adaptive echo cancellation circuit, resulting a higher component cost. In the case that the transformer inductance L is too small, the transformer imposes distortion on the receive signal from the line, thereby deteriorating the function of the receiver.

The digitized signal is taken to a summing point 6, where it is summed for echo cancellation with the inverted receive signal taken from the transmitter 1 via an adaptive FIR filter. Thus, a signal component processed by the filter 7 is subtracted from the receive signal in order to cancel the transmit signal echo, whereby the output 20 of the summing stage 6 delivers the echo-free modem output signal.

By denoting the resistance 17 with symbol R for the sake of simplicity, the transfer function of a circuit configuration according to the prior art can be computed from the diagram of Fig. 1:

$$\frac{V_o}{V_i}=\frac{sL\|Z_L}{R+sL\|Z_L}=\frac{1}{1+\frac{R}{sL\|Z_L}}=\frac{1}{1+R(\frac{1}{sL}+\frac{1}{Z_L})} \qquad (1)$$

This equation may further be written:

$$\frac{V_o}{V_i}=\frac{s}{s(1+\frac{R}{Z_L})+\frac{R}{L}} \qquad (2)$$

In the circuit configuration according to the invention illustrated in Fig. 2, the feedback path is formed by means of an integrator 9 from the connection point of the line drive impedance 17 and the primary winding of the transformer 8 to the input of the transmitter buffer 3.

As the integrator 9 represents a term -A/s, the transfer function of the circuit configuration according to the invention comprising the integrator 9 may be written from point V_x to point V_o as follows:

$$V_x = V_i - \frac{A}{s} \cdot V_o \qquad (3)$$

This equation may further be rewritten:

$$V_o = \frac{Z}{R+Z} \cdot V_x = \frac{Z}{R+Z} [V_i - \frac{A}{s} \cdot V_o] \qquad (4)$$

Rewriting the equation gives:

$$(1 + \frac{A}{s} \cdot \frac{Z}{R+Z}) V_o = \frac{Z}{R+Z} \cdot V_i \qquad (5)$$

which may be further rewritten as:

$$\frac{V_o}{V_i} = \frac{\frac{Z}{R+Z}}{1 + \frac{A}{s} \cdot \frac{Z}{R+Z}} = \frac{sZ}{s(R+Z) + AZ} \qquad (6)$$

When the resultant impedance Z is divided into a parallel connection of the transformer impedance L and the line impedance Z_L in the following manner:

$$\frac{1}{Z} = \frac{1}{sL} + \frac{1}{Z_L} \qquad (7)$$

which the transfer function can be written as:

$$\frac{V_o}{V_i} = \frac{s}{s(1+\frac{R}{Z})+A} = \frac{s}{s(1+\frac{R}{sL}+\frac{R}{Z_L})+A} \qquad (8)$$

which may further be rewritten as:

$$\frac{V_o}{V_i} = \frac{s}{s(1+\frac{R}{Z_L})+\frac{R}{L}+A} \qquad (9)$$

A comparison of the transfer functions represented by Eqs. 2 and 9 reveals that Eq. 9 can be rewritten as:

$$\frac{V_o}{V_i} = \frac{s}{s(1+\frac{R}{Z_L})+\frac{R}{L}\cdot(1+\frac{AL}{R})} \qquad (10)$$

Here, the transformer inductance is seen to be virtually reduced to a value of:

$$L \to \frac{L}{1+A\cdot\frac{L}{R}} \qquad (11)$$

Obviously, the coefficient A of the integrator 9 can be used for controlling said inductance.

The integrator 9 can be implemented in a plurality of alternative methods either using a continuous-signal operational amplifier or a discrete-signal filter known in the art as the "switched-capacitor circuit", whereby the coefficient A may be easily adjusted.

In Fig. 3 is shown a continuous-signal operational amplifier configuration, in which the time constant RC is the inverse of the coefficient A. Hence, the circuit 9 of Fig. 3 comprises an operational amplifier 10 having its output terminal connected via a capacitor 11 to the inverting input of the operational amplifier 10. A resistor 12 with a capacitor 11, both connected to the inverting input terminal of the amplifier, determine the integration time constant of the integrator. Thus, said time constant is a product of said components, and therefore, the inverse of said coefficient A.

In practice, the coefficient A is adjusted by, e.g., selecting the value of the resistance 12 according to the modem data transfer speed from a resistor matrix (by means of solid-state switches, for instant). Then, the value of the capacitor 11 is kept unchanged. Alternatively, the capacitor 11 can be selectable from a switched capacitor matrix, whereby the value of the resistor 12 is kept unchanged.

In Fig. 4 is shown an integrator embodiment implemented using the "switched-capacitor" technique, in which the value of KC_2/C_1 is the inverse of the coefficient A. Herein, K is a coefficient dependent on the frequency of the clocks driving the solid-state switches SW1-SW4. In the diagram, Φ_1 and Φ_2 denote clock signal of opposite phase that control the solid-state switches SW1-SW4. Thence, the coefficient A can be altered by either changing said clock frequency or implementing the

capacitors C_1 and C_2 as a capacitor matrix controlled by solid-state switches.

Claims:

1. A circuit configuration for adapting an echo-cancelling multispeed modem to a line, said circuit comprising

- a transmitter (1),

- a transmitter buffer (3) connected on the signal path of the transmitter (1),

- a line drive resistance (17) connected to the output of the transmitter buffer (3),

- a line transformer (8) connected to the line drive resistance (17), and

- echo-cancelling elements (5, 6, 7) for eliminating the transmit signal echo from the receive signal,

c h a r a c t e r i z e d in that

- to the input of the transmitter buffer (3) is arranged a feedback path from the connection point of the line transformer (8) and the line drive resistor (17) by means of an integrator (9).

2. A circuit configuration as defined in claim 1, c h a r a c t e r i z e d in that said integrator (9) is implemented by means of continuous-signal operational amplifier circuit having the time constant (A) of the integrator (9) made controllable.

3. A circuit configuration as defined in claim 1, c h a r a c t e r i z e d in that said integrator (9) is implemented by means of discrete-signal operational amplifier circuit having the time constant (A) of the integrator (9) made controllable.

4. A circuit configuration as defined in claim 1, c h a r a c t e r i z e d in that the time constant control of said integrator (9) is implemented by means of a resistor or capacitor matrix controlled by solid-state switches.

5. A circuit configuration as defined in claim 1, c h a r a c t e r i z e d in that said integrator (9) includes a controllable resistor (12) for setting the time constant of said integrator.

6. A circuit configuration as defined in claim 1, c h a r a c t e r i z e d in that said integrator (9) includes a controllable capacitor (11) for setting the time constant of said integrator.

7. A circuit configuration as defined in claim 3, c h a r a c t e r i z e d in that said integrator (9)

includes a controllable capacitor (C_1 or C_2) for setting the time constant of said integrator.

8. A circuit configuration as defined in claim 3, c h a r a c t e r i z e d in that said integrator (9) includes a means for controlling the clock frequency of said controllable switches (SW1-SW4).

9. A method of adapting such an echo-cancelling multi-speed modem to a line which modem comprises

- a transmitter (1),

- a transmitter buffer (3) connected on the signal path of the transmitter (1),

- a line drive resistance (17) connected to the output of the transmitter buffer (3),

- a line transformer (8) connected to the line drive resistance (17), and

- echo-cancelling elements (5, 6, 7) for eliminating the transmit signal echo from the receive signal,

c h a r a c t e r i z e d in that

- to the input of the transmitter buffer (3) is arranged a feedback path from the connection

point of the line transformer (8) and the line drive resistor (17) by means of an integrator (9).

10. A method as defined in claim 9, c h a r a c t e r i z e d in that said integrator (9) is implemented by means of continuous-signal operational amplifier circuit having the time constant (A) of the integrator (9) made controllable.

11. A method as defined in claim 9, c h a r a c t e r i z e d in that said integrator (9) is implemented by means of discrete-signal operational amplifier circuit having the time constant (A) of the integrator (9) made controllable.

12. A method as defined in claim 9, c h a r a c t e r i z e d in that said integrator (9) includes a controllable resistor (12) for setting the time constant of said integrator.

13. A method defined in claim 9, c h a r a c t e r i z e d in that said controllable resistor (12) is an electronically switched resistor matrix.

14. A method as defined in claim 9, c h a r a c t e r i z e d in that said time constant (A) is controlled by altering the clock frequency of said controllable switches (SW1-SW4).

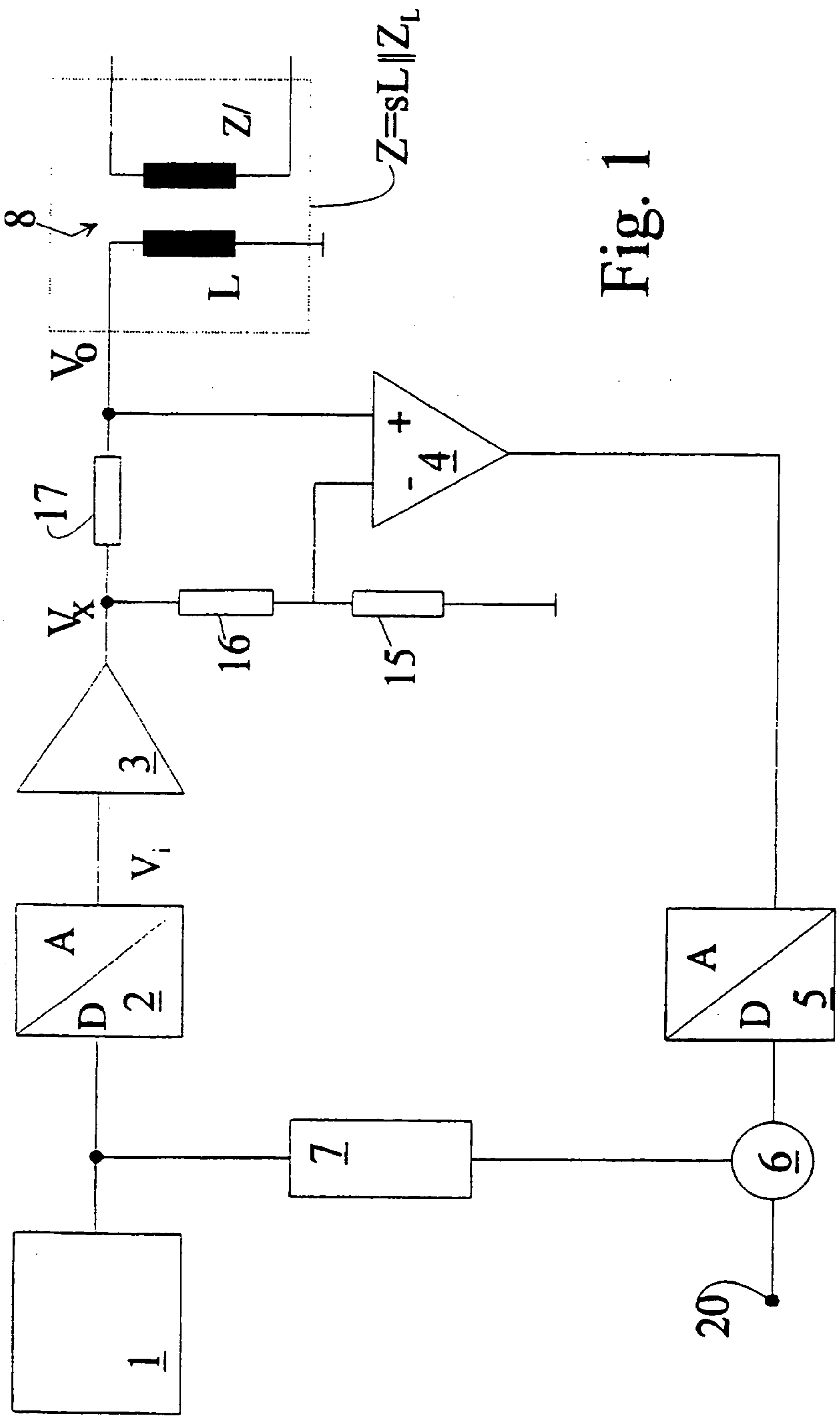

Fig. 1

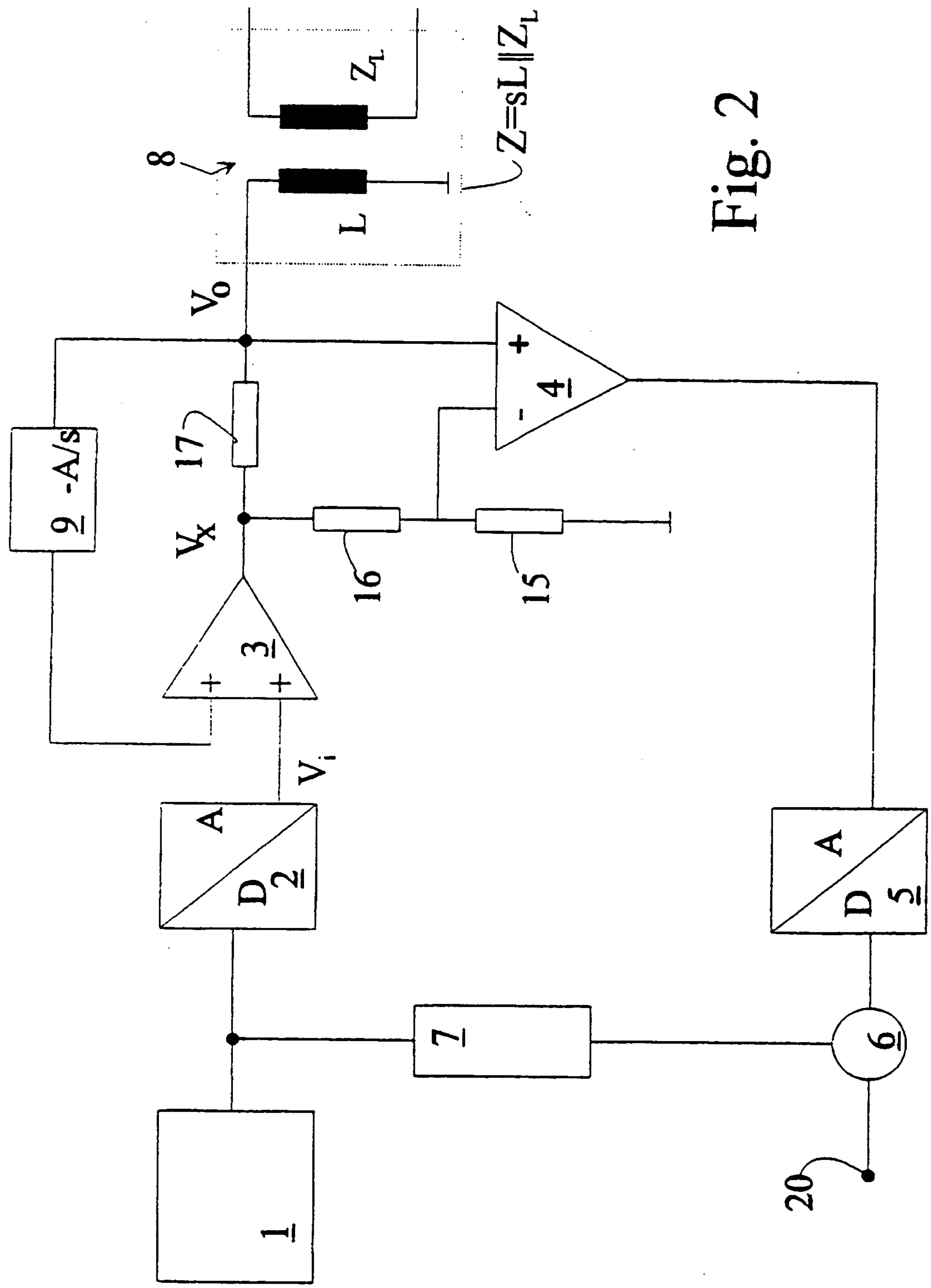

Fig. 2

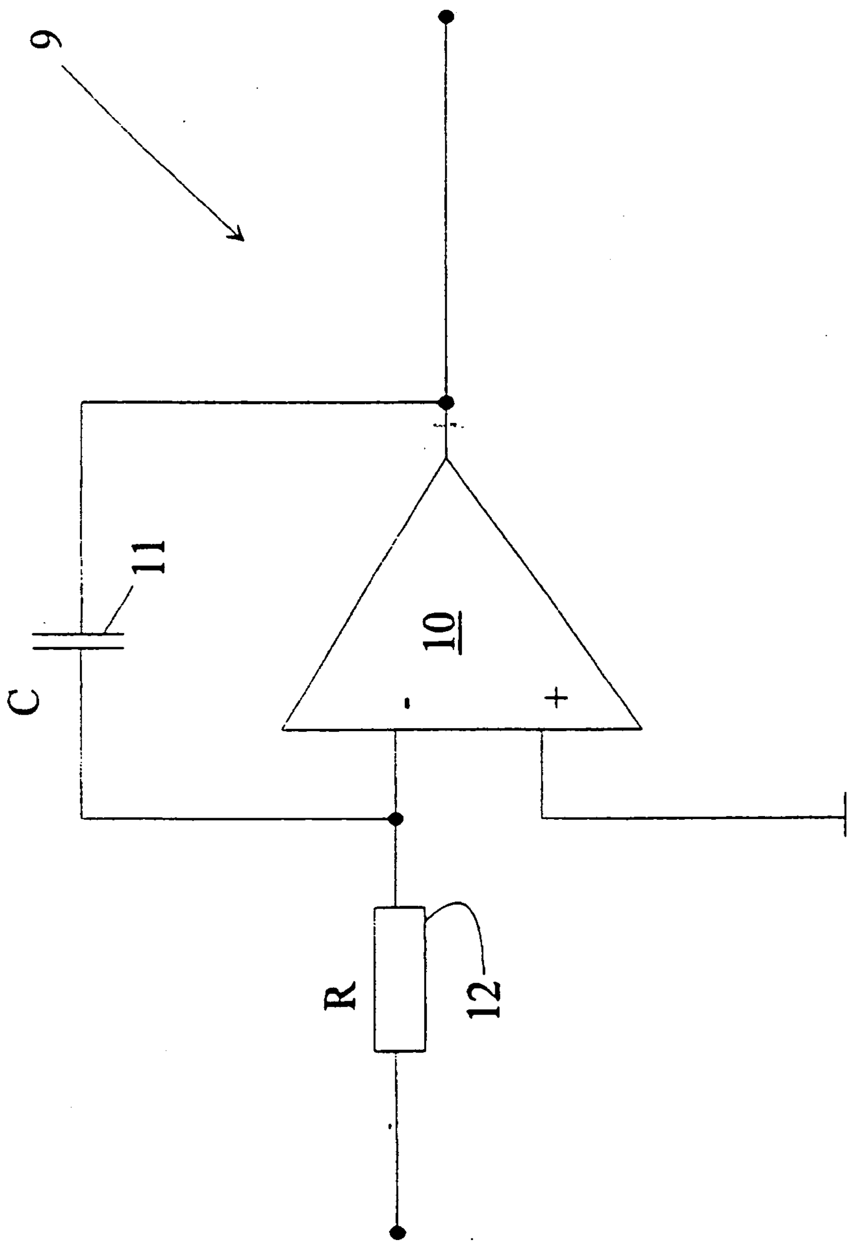

Fig. 3

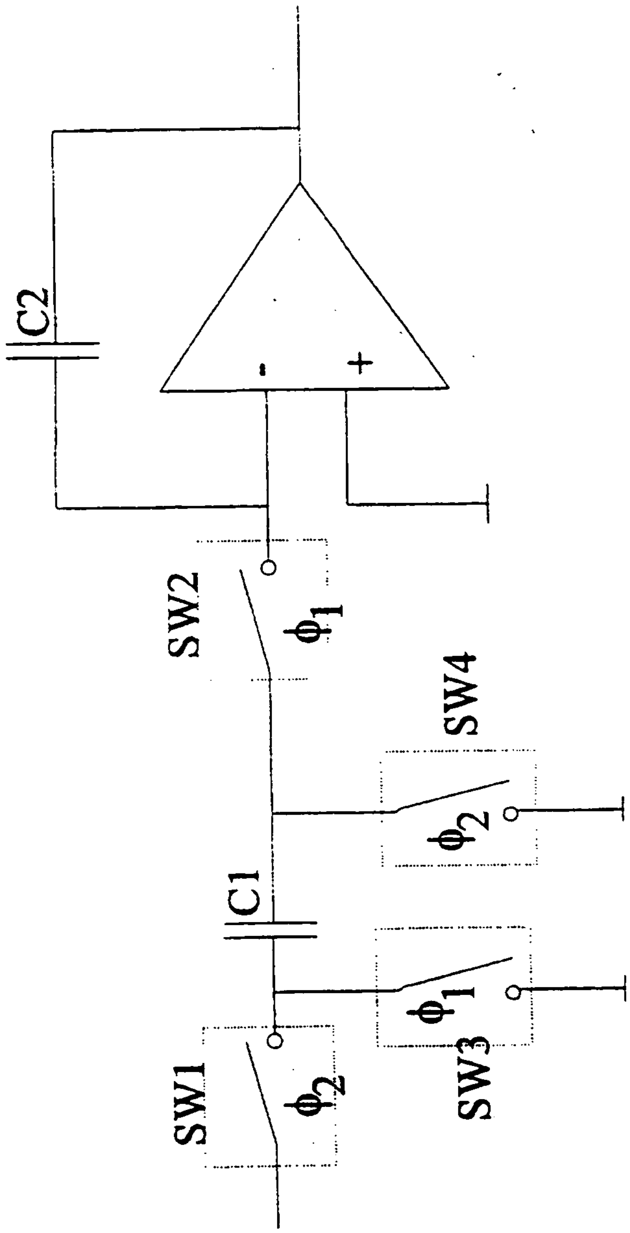

Fig. 4

INTERNATIONAL SEARCH REPORT

International application No.
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A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H04B 3/23, H04B 3/03, H04M 11/06

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0691771 A2 (ROCKWELL INTERNATIONAL CORPORATION), 10 January 1996 (10.01.96), column 4, line 11 - line 37; column 8, line 12 - line 51, figure 3	1-14
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A	US 4888762 A (MASANOBU ARAI), 19 December 1989 (19.12.89), figures 1,3,5, see the whole document	1-14
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A	US 5222084 A (YUTAKA TAKAHASHI), 22 June 1993 (22.06.93), column 1, line 12 - line 68; column 2, line 1 - line 68; column 3, line 1 - line 48, figure 3	1-14
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[X] Further documents are listed in the continuation of Box C. [X] See patent family annex.

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C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

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A	US 5204854 A (ROUBIK GREGORIAN ET AL), 20 April 1993 (20.04.93), figure 6, Detailed description --	1-14
A	US 5371789 A (AKIHIRO HIRANO), 6 December 1994 (06.12.94), see the whole document -- --------	1-14

INTERNATIONAL SEARCH REPORT

Information on patent family members

03/02/98

Inter ional application No.
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